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LOW POWER DELAY PRODUCT FULL ADDER DESIGN USING PASTA AND PTL CMOS LOGIC

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ABSTRACT

The design of Full Adder circuit using Multiplexer (Mux) based Parallel self-Timed Adder (PASTA) and Mux based Pass Transistor Logic (PTL) is designed using CMOS. Both the adder circuits are implemented in 130-nm CMOS technology process which aims at the current flows from source to drain should be high. The power, delay and the power delay product (PDP) are obtained by using T-spice simulation. The simulation results show that the Mux based PTL adder circuit provides lower PDP than the Mux based PASTA adder circuit.

Keywords: CMOS, PASTA, PTL, Multiplexer, PDP

I INTRODUCTION

Adder is a digital circuit which is used to perform addition of numbers mostly in bit-wise manner. Binary addition operation plays a vital role in the processor performance. Based on the inputs, adders are designed using synchronous circuits (clock) than asynchronous circuits (clock less). But a clock circuit undergoes more drawbacks than clock less circuits such as high power consumption and more Electro Magnetic Interference (EMI). Asynchronous circuits consume power only when the operation performs. Asynchronous circuits provide less noise and errors due to less EMI [5]. By controlling the data transfer protocol in this circuit, pipeline is established in the absence of clock. Since bit adders are expensive, dual-rail carry propagation is used to efficiently manage the adders. The acknowledgement is provided by the dual-rail carry output from the single bit adder block. Thus, it is either based on the full dual-rail encoding of all signals or pipelined

operation. This provides robustness to the circuits and average case performance is significantly improved [2].Self-timed circuits uses request-acknowledgement protocol to transfer data between the modules of the circuit and hence it avoids timing problem. Self-timed circuits uses completion signals for data transfer control. The completion signal can be generated by Differential Cascode Voltage Switch (DCVS) logic. This is dual-rail coded logic which will generate completion signals when computational operation has finished. DCVS logic undergoes several advantages over other CMOS logic such as speed, power, logic flexibility and it has specific inherent self- testing property .The disadvantage of this logic is that it requires larger area for routing and the design of this logic is very difficult due to lack of supporting design tools [3]. A Domino gate consists of an N -Block gate stage, a static CMOS inverter and a PMOS keeper transistor. The static CMOS inverter is used to drive the circuit's output, and it enhances the speed of Domino logic. The PMOS keeper circuit is used to restore the logic at the Domino output node. When CLK is low, the keeper transistor is turned ON and the Domino node is charged to VDD. Depending on the inputs, the Domino node either discharges to ground or remains high at VDD when clock input is high [4]. Delay Insensitive Adders are asynchronous adder that uses dual-rail encoding which increases the complexity but still has the capability to produce the circuits that are efficient than single-rail encoding by using NMOS designs. PASTA is a design of full adder circuit by using MUX and half adder. Recursive approach is used in this logic [1]. DI adders have many variants like DI ripple carry adder, DI carry look ahead adder. The variants of the DI adders also use dual-rail encoding [6]. Conventional CMOS are designed by using P block and N block. When the state is '0',N block gets evaluated likewise when the state is '1',P block gets evaluated. Hence one block will be conducting depending upon the state. Conventional CMOS has several advantages such as robustness reliability and small transistor sizes. The drawback of this CMOS logic is it has weak output driving capability and it has low mobility due to the presence of P block [4].

This paper is summarized as follows. Section II deals with the design of Mux based PASTA adder circuit design. The Mux based PTL adder is discussed in Section III. The simulation results are summarized in section IV and finally it is concluded in section V.

II DESIGN OF MUX BASED PASTA

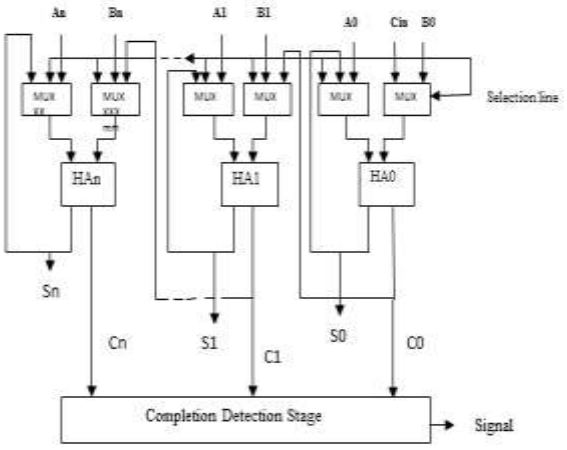

Figure.1 Design of n-bit PASTA using Mux

The figure.1 represents the n-bit Parallel Self-Timed Adder circuit. It consists of multiplexer and half adder circuits.When the selection line is 0,the bit A0 and B0 are

taken as input to the multiplexer block.The output of the multiplexer block is given as input to the half adder block.The output sum (S0,S1,……Sn) is obtained by performing XOR operation in the half adder circuit and carry is obtained by performing AND operation. The carry bit obtained from previous bit is given as the input to the multiplexer of the next bit.The value of sum that is obtained is again given as input to the multiplexer.The value of sum is taken as input along with Cin when the selection line is 1. Recursive iterations will continue until all the carry signals is assumed to zero values. The completion detection stage is the activation signal collects all the carry bits and the output is termed as signal.

For n block circuit the value of sum and carry for i^{th} bit and k^{th} iteration,

$$S_i^0 = A_i \text{ xor } B_i$$

$$C_{i+1}^0 = A_i.B_i$$

For n block circuit the C_{n+1}^k and S_i^k is the carry for i^{th} bit at the k^{th} iteration

$$S_i^k = S_i^{k-1} \text{ xor } C_i^{k-1}, \text{ for } 0 \leq i \leq n$$

$$C_{i+1}^k = S_i^{k-1}.C_i^{k-1}, \text{ for } 0 \leq i \leq n$$

III. DESIGN OF MUX BASED PTL

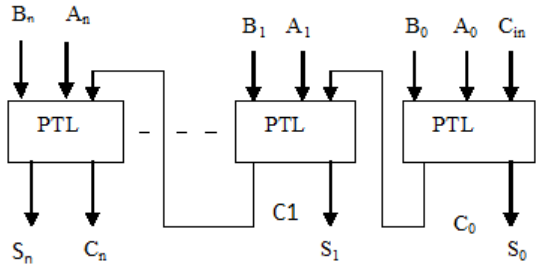

Figure.2 Design of n-bit PASTA using Mux

The figure.2 represents the n-bit pass transistor logic circuit.The single PTL block consists of two multiplexer, two inverter and one NMOS transistor. Pass Transition Logic (PTL) reduces the number of transistor which access the input as output.By depending upon the value of A and B, the value of sum can be obtained.If both the value of A and B are equal, the value of C_{in} will be taken as the value of Sum.If the value of A and B are not equal, then the value of sum will be the invert of the value of C_i. The carry output of the previous bit is given as input to the next bit.The circuit is designed in such a manner that the value of carry bit depends upon the value of A and C_i.In a single bit PTL design,when the value of A is 1,it enables the NMOS transistor and the current will flow from source and the value of sum can be obtained.Similarly, when the value of B is 1 it enables the NMOS transistor present at the inverter block.When the value of C_i is 1,it enables the NMOS at the multiplexer design and the value carry can be obtained.

IV SIMULATION RESULTS

The full adder circuit is designed and implemented using Tanner EDA tool. The simulation results are obtained in 130nm CMOS technology process. The figure.3 shows the simulated waveform of 2-bit Parallel Self-Timed Adder.

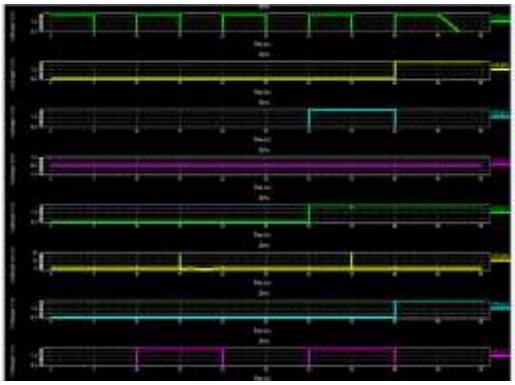

Figure.3 Simulated Waveform of 2-bit Full Adder using Mux based PASTA

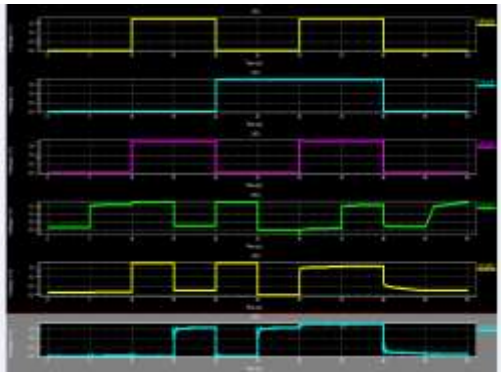

Figure.4 Simulated Waveform of 2-bit Full Adder using Mux based PTL

The simulation result is obtained under recursive approach of the carry and sum. The value of selection line is continuously varied as 0 and 1.Depending upon the value of the selection line, the input is taken and it is processed. The value of sum is obtained by performing XOR operation and the value of carry is obtained by performing AND operation.Since it is a two bit adder A_0, B0, A1, B1 are taken as input. When the Selection line is 0, the values of A_0,B_0 and A_1,B_1 are processed parallely and the value of sum and carry is obtained. The value of sum obtained is again given as input to the mux and the value of carry is given as input to the mux at the next bit. When the selection line is 1, the value of previous sum and C_{in} is taken as input at the first bit. Similarly at the second bit ,the previous bit carry and sum is taken as input and recursively sum and carry are obtained.

The figure.4 represents the simulated waveform of 2-bit full adder using Mux based PTL. This design consists of inputs such as A_0,B_0, A_1,B_1 and C_i. When A_0 and B_0 are equal the value of sum will be same as that of the value of C_i. If A_0 and B_0 are not equal, the value of sum will be the invert of C_i. The value of carry is obtained depending upon the value of A and C_i. The value of the carry is send as the input to the next single bit PTL design. Similarly at the next PTL circuit the value of sum is obtained depending upon the value of A_1,B_1. When A_0 and B_0 are equal the value of sum will be same as that of the value of carry obtained from the previous PTL design.

Table.1 Comparison of Full Adder circuit Designs using Mux based PASTA and Mux based PTL

Parameters	2-Bit Adder		4-Bit Adder		8- Bit Adder	
	PASTA	PTL	PAST	PTL	PASTA	PTL
Power (mW)	4.8	2.4	10.7	4.88	18	9.75
Time (µs)	20	10	20	15	15	15
PDP (nW/s)	96	24	214	73	270	146.2

The table.1 represents the simulated results of 2-bit, 4-bit, 8-bit full adder design using Mux based PASTA and Mux based PTL CMOS logic circuits. Form this table it os observed that the Mux based PTL logic provides the better PDP than the Mux based PASTA logic circuit.

V CONCLUSION

The full adder circuits are designed using Mux based PASTA and Mux based PTL logic circuits. The full adder circuits are implemented in 130nm CMOS technology process. The Power, Delay and PDP of 2-bit, 4-bit, and 8-bit full adders are obtained and their results are compared. Simulated results show that Mux based PTL full adder provides lower PDP compared to the Mux based PASTA full adder.

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